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10/053,685	01/24/2002	Pavan M. Kumar	PW 276911 P12610	8409

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ROGER R. WISE, ESQ.
PILLSBURY WINTHROP LLP
725 SOUTH FIGUEROA STREET
SUITE 2800
LOS ANGELES, CA 90017-5406

EXAMINER
NGUYEN, DANNY

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,685	KUMAR ET AL.	
	Examiner	Art Unit	
	Danny Nguyen	2836	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,13-19 and 22-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,17,18,24,25,30* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 7-12, 20, 21, 31, and 32 are cancelled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-5, 19, 22-23, 26-29 are rejected under 35 U.S.C. 102(a) as being anticipated et al. by Muratov et al. (Publication Number 2001/0045815).

Regarding to claim 1, Muratov et al. disclose a power supply system (see fig. 2) comprise a controller (including PWM circuit, 50 and 60) to cause regulator (100) to produce a principle supply voltage (when the processor in performance operating mode) and secondary supply voltage (when the processor in battery mode, see table 2), the regulator (100) for coupling to a power source (Vin) and to a micro-electronics device (note-book computer) to supply the a principle supply voltage and secondary supply voltage to the micro-electronic device (processor);and wherein the controller is further to maintain the principle supply voltage with in a tolerance window (within 2.5% tolerance) and maintain the secondary supply voltage in the second tolerance level (2.5% tolerance), and the first reliability voltage is determined by multiplying one plus a tolerance level by a first input voltage required value (1.6 * (1 + (-) 2.5) = 1.64 or 1.56V as shown in table 2).

Regarding to claim 2, Muratov et al. disclose the controller causes the regulator to produce a third supply voltage and maintain the third supply voltage with a third tolerance level (see 0023).

Regarding to claims 3-5, Muratov et al. disclose the principle supply voltage and the second supply voltage (voltage in performance mode and voltage in battery-optimized mode) are determined in accordance a gain factor (determined by current gain circuit 72) in accordance with a voltage-current load line and the voltage current load line specifies a total power voltage current load line (voltage-current load line shown in fig. 3).

Regarding to claim 19, Muratov et al. disclose a microelectronic device (note-book computer) having at least two input voltage required values to receive at least two input supply voltage (such as shown in table 2), a regulator (100) coupled to the device and power source (Vin) connected to the regulator circuit (100) wherein the regulator produces the at least two supply voltages (voltage in performance mode and voltage in battery-optimized mode) within an input range bounded by an upper limit and lower limit (with 2.5% tolerance), wherein the upper limit of each of the two input supply voltage is a first reliability voltage value (+2.5% *1.6 + 1.6 V = 1.64V), and the lower limit determined by the gain factor (gain circuit 72) multiplied by each of the two input supply voltages (see 001).

Regarding to claim 23, Muratov et al. disclose the regulator determines the gain factor (by gain circuit 72) for each of the at least two input supply voltages according to a voltage-current load line (shown in fig. 3), and the lower limit of the at least two input

supply voltages is equal to the product of one point four minus a tolerance level multiplied by a corresponding to one of the two input supply voltages (1.35 –2.5%*1.35 which is shown in table 2).

Regarding to claims 26, 27, Muratov et al. disclose a regulating method comprises the steps of supplying multiple input voltages (voltage in performance mode and voltage in battery-optimized mode) to microelectronic device (note-book computer), determining an upper limit of the first voltage regulation range equals to (1.6 * (1 + 2.5%)) = 1.64 V as shown in table 2, and for the second voltage value, the upper limit equals to ((1.35 * (1 + 2.5%)) = 1.384V as shown in table 2, determining a lower limit of the voltage regulation according to a voltage-current load line (1.35 –2.5%*1.35 which is shown in table 2 and fig. 3), maintaining each of the multiple input supply voltages to the microelectronic devices (note-book computers) above the lower limit and under the first reliability voltage (such as 2.5%*1.6 + 1.6).

Regarding to claims 28, 29, Muratov et al. disclose the step of selecting a gain factor (determined by current gain circuit 72) to produce multiple input voltages in accordance with a voltage-current load line and the voltage current load line specifies a total power voltage current load line (voltage-current load line shown in fig. 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 13-16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Siri (USPN 6,009,000) in view of Muratov et al.

Regarding to claims13, 14, Siri discloses a regulator (see fig. 2) comprises a plurality of regulator circuits (30a and 30b), each the regulator circuit (30a) for coupling to a load (12), wherein the each regulator circuit provides a particular one of the regulated input voltages (Vo1 and V02, see fig. 2) to the load (12). Wherein each regulator further includes a controller (32c) including a comparator (80a) and a threshold detector (86a and 91a), an input of the comparator connected to an output of the threshold detector, a switch (78) coupled to the controller and operating in response to a signal provided by the controller, the switch being connected to an inductor (74), a diode (75), and an output capacitor (76) arranged in a network that produces a load current (lo1 and l02) in response to an input voltage received via the switch, the controller maintains the one of regulated input voltages within a level tolerance (within 1% tolerance, see col. 3, lines 18-21). Siri does not disclose the load being a micro-electronic device; the current feedback control loop having a gain factor and the controller maintains regulated input voltages in accordance to voltage current load line. Muratov et al. disclose the load being a notebook computers (see 0002), the feedback control loop having a gain factor and the controller maintains the regulated input voltage in accordance to a voltage-current load line (see fig. 2 and table 3). It would have been obvious to one having skill in the art at the time the invention was made to combine the regulator circuit of Siri with a load being an electronic device, gain factor and controller

maintains the regulated input voltages in accordance to a voltage-current load line in order to adjust droop to match and compensate for changes in operation modes.

Regarding to claims 15-16, Siri discloses all limitations of claim13 except for having the voltage-current load line specifies a linear relationship and the voltage current load line is a total power voltage current load line. Muratov et al. disclose the voltage-current load line specifies a linear relationship and the voltage current load line is a total power voltage current load line (see fig. 3). It would have been obvious to one having skill in the art at the time the invention was made to combine the regulator circuit of Siri with a load being an electronic device, gain factor and controller maintains the regulated input voltages in accordance to a voltage-current load line in order to adjust droop to match and compensate for changes in operation modes.

Response to Arguments

4. Applicant's arguments filed 7/7/2003 have been fully considered but they are not persuasive.

Regarding to claims 1, 19, applicant argued that the Muratov et al reference do not disclose or teach the first reliability voltage is determined by multiplying one plus a tolerance level by a first input voltage required value. Examiner respectfully disagrees with the argument. Muratov disclose that the first reliability voltage is determined by multiplying one plus a tolerance level by a first input voltage required value (1.6 * (1 + (-) 2.5) = 1.64 or 1.56V as shown in table 2). Thus, the applicant's arguments of the amended claims 1 and 19 do not overcome the Muratov reference.

Regarding to claim 26, applicant argued that the Muratov et al reference do not disclose or teach determining an upper limit of the voltage regulation range for all of the multiple input voltages by multiplying a first corresponding input voltage required value by sum of one plus a tolerance level. However, Mutatov disclose a regulation system (such as shown in fig. 2) operating with two different voltage level (such as 1. 6V and 1.35V) having a tolerance 2.5%. Those having skilled in the art would realize that for the upper limit of the first voltage regulation range equals to (1.6 * (1 + 2.5%)) = 1.64 V as shown in table 2, and for the second voltage value, the upper limit equals to ((1.35 * (1 + 2.5%)) = 1.384V as shown in table 2, Thus, the applicant's arguments of the amended claim 26 do not overcome the Muratov reference.

Regarding to claim 13, applicant argued that the combination of Siri and Muratov et al references do not disclose or teach plurality of regulator circuits and the plurality of regulated input voltages being maintained within voltage bounded at an upper limit by a first reliability voltage value, whereby the first reliability voltage is determined by multiplying a first one of the plurality of input voltages by the sum of one and a tolerance level as amended in claim 13, However, Siri teaches plurality of regulator circuits (30a and 30b shown in fig. 2) and Muratov discloses the plurality of regulated input voltages (1.6V and 1.35V) being maintained within voltage bounded at an upper limit (+2.5%) by a first reliability voltage value, whereby the first reliability voltage is determined by multiplying a first one of the plurality of input voltages by the sum of one and a tolerance level (1.6 * (1 + 2.5%)) = 1.64V. Therefore, the applicant's arguments of the amended claim 13 do not overcome the combination of Siri and Muratov.

Allowable Subject Matter

5. Claims 6, 17, 24, 25, 30 are allowed.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (703)-305-5988. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703)-308-3119. The fax phone numbers for the organization where this application or proceeding is assigned are (703)-872-9318 for regular communications and (703)-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-308-0956.

DN

DN
September 15, 2003

GREGORY J. TOATLEY, JR.
PRIMARY EXAMINER